Single Electron Transistors with Quantum Wires

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With the recent rapid progress of fabrication techniques for nanostructures, many types of single-electron transistors have been fabricated. Most single electron transistors have been fabricated from two dimensional electron gas systems by using split gate technique to form a dot structure. The dot structure is realized completely by applying negative biases on all the gates around the dot. This limits its application on super-sensitivity to charge. We have developed a new technique to fabricate novel single electron transistors, which is suitable for the following applications: 1) control single electron process in single electron memories, 2) probe edge states in quantum hall effects, 3) monitor logic operations in single electron logical circuits (including quantum dot cellular automata), 4) make clear whether coherent tunneling or sequential tunneling dominate the transport in two dot structures. In addition, in-plane gates are used in fabricating of single electron transistors instead of split gates, which made the devices work at higher temperatures. From engineering viewpoint, these single-electron transistors have more chances to be used to construct next-generation electronics with new system architectures. These transistors are not only suitable for their integration but also have potential applications in investigating quantum effects. Efforts have been paid to raise their working temperatures. The operation at room temperature for such kinds of devices has also been reported. However, some of these devices have showed complicated behaviors because of the formation of multiple-dots in the wire channels. The realization of the high-temperature operation for these devices is mainly dependent on the channel widths. As the channel width is decreased, the fluctuation of the geometric width becomes more serious. This leads to the formation of multiple-dots. Therefore, it is very important to develop some techniques which can be used to realize one single dot in the narrow channels. We have combined in-plane gate technique and split gate technique and developed them into nanelectrode-pair technique. We have further developed such a technique by a self-aligned process to fabricate Si single electron transistors with in-plane point-contact metal gates. The characteristics of such single electron transistors strongly depend on the channel widths and the voltages on the in-plane gates. Applying a negative voltage to the in-plane gates squeezes the narrow channel. The electrical field at the center of the in-plane gates is the strongest because of the smallest separation between the gates. This facilitates realizing a single dot at the center of the channel. This technique could also be very helpful in fabricating high-temperature SETs from self-assembled dot structures.

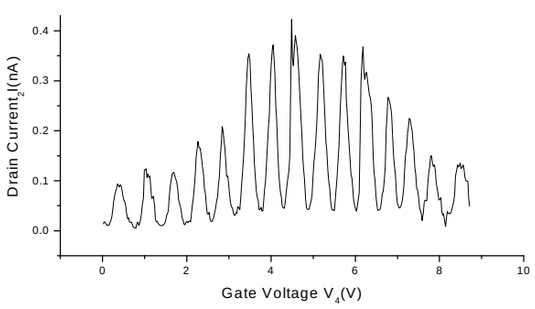

Fig. 1 shows Coulomb blockade oscillations from one device with 30nm-wide wire. The modulation of the amplitude in the oscillations is attributed to the quantum interference effect.